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L1 710/100,300,306,313,301,105;709/252,301;361/683,686,724;370/400,465,522,408.ccls. 11376 L1

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L1 and L3	22

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<u>L4</u>	l1 and L3	22	<u>L4</u>
<u>L3</u>	L2 and ((card or board) near5 (CPU or processor))	140	<u>L3</u>
<u>L2</u>	CPCI or "compact peripheral component interconnect"	337	<u>L2</u>
<u>L1</u>	710/100,300,306,313,301,105;709/252,301;361/683,686,724;370/400,465,522,408.ccls.	11376	<u>L1</u>

END OF SEARCH HISTORY

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L5 and (first same second)	39

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<u>L6</u>	15 and (first or second)	50	<u>L6</u>
<u>L5</u>	L2 same ((card or board) same ("operating system" or OS)) same (CPU or processor)	51	<u>L5</u>
<u>L4</u>	L2 same ((card or board) same ("operating system" or OS))	78	<u>L4</u>
<u>L3</u>	L2 and ((card or board) same ("operating system" or OS))	161	<u>L3</u>
<u>L2</u>	CPCI or "compact peripheral component interconnect"	337	<u>L2</u>
L1	CPCI or "compact peripheral component interconnect"	322	L1

END OF SEARCH HISTORY

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DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L8 L70 L8

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L7 15 and (first same second)39 L7L6 15 and (first or second)50 L6L5 L2 same ((card or board) same ("operating system" or OS)) same (CPU or processor)51 L5L4 L2 same ((card or board) same ("operating system" or OS))78 L4L3 L2 and ((card or board) same ("operating system" or OS))161 L3L2 CPCI or "compact peripheral component interconnect"337 L2~~L1 CPCI or "compact peripheral component interconnect"~~~~322 L1~~

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11 same ((CPU or processor) near5 (card or board))

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1	<input type="checkbox"/>	<input type="checkbox"/>	US 6898278 B1	20050524	22	Signaling switch for use in information prot	379/325	379/229
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6889245 B2	20050503	11	Tightly-coupled disk-to-CPU storage ser	709/203	709/238; 711/114
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6882311 B2	20050419	13	Digital beamforming radar svstem	342/368	455/318
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6865637 B1	20050308	10	Memory card and system for updating distribute	710/305	700/20; 700/5;
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6853551 B2	20050208	21	Telecommunication chassis	361/687	345/519; 361/722;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6836811 B2	20041228	11	Front access only CPCI computer svstem	710/301	361/788; 710/105
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6785840 B1	20040831	15	Call processor system and methods	714/11	710/305; 714/4
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6731741 B1	20040504	31	Signaling server for processing signaling in	379/221.08	379/230; 379/900
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6724635 B2	20040420	13	LCD panel for a server svstem	361/736	361/679; 361/681
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6721411 B2	20040413	16	Audio conference platform with dvnamic s	379/202.01	370/263; 379/201.0
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6678281	20040113	11	Hardware configuration,	370/438	370/463



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» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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Article Information

**1. Evolution of digital signal processing based spacecraft computing solutions**

Persyn, S.C.; McClelland, M.; Epperly, M.; Walls, B.;
Digital Avionics Systems, 2001. DASC. The 20th Conference
Volume 2, 14-18 Oct. 2001 Page(s):8C3/1 - 8C3/10 vol.2

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**2. Onboard processor for compressing HSI data**

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Kemmerling, G.; Engels, R.; Bussmann, N.; Clemens, U.; Heiderich, M.; Reinartz, R.; Rongen, H.; Schelten, J.; Schwahn, D.; Zwoil, K.;
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Volume 48, Issue 4, Aug. 2001 Page(s):1114 - 1117











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Volume 5, 10-17 March 2001 Page(s):2199 - 2207 vol.5

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Clatene, A.
Motorola Inc., Sunnyvale, CA, USA ;This paper appears in: **Aerospace Conference, 1998. Proceedings., IEEE**

Publication Date: 21-28 March 1998

Volume: 4

On page(s): 505 - 514 vol.4

Number of Pages: 5 vol. (xxii+494++516+500+568+552)

Meeting Date: 03/21/1998 - 03/28/1998

Location: Snowmass at Aspen, CO

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DOI: 10.1109/AERO.1998.682217

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Abstract

The Peripheral Component Interconnect (PCI) bus is an important and critical component of high performance workstations and embedded systems. Most embedded system architecture designs are based on more than one bus scheme which include a host processor bus and/or other bus schemes such as VMEbus, Industry Standard Architecture (ISA), Enhanced Industry Standard System Architecture (EISA) or a PCI bus. The PCI bus provides the wide bandwidth needed to support the high performance requirements for embedded systems applications. This paper examines bus bandwidth requirements for high performance embedded systems and a brief discussion of the benefits of the PCI bus. Applications solutions for the PCI bus in embedded systems with particular emphasis on high speed I/O data communications and networking systems are reviewed. Advanced approaches in moving I/O functionality and intelligence from the host computer to logical subsystems via the new industry specification for intelligent I/O (I2O) are also examined

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Non-controlled Indexing

Industry Standard Architecture ECLbus VMEbus embedded system architecture high performance workstations high speed I/O data communications high speed I/O systems host computer host processor bus industry specification intelligent I/O logical subsystems networking peripheral component interconnect bus wide bandwidth

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May 19, 2005

PGPUB-DOCUMENT-NUMBER: 20050108573

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050108573 A1

TITLE: Real-time network monitoring and security

PUBLICATION-DATE: May 19, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Bennett, Mark Arwyn	Surrey		GB	
Piggott, Alexander Colin	Surrey		GB	
Garfield, David John Michael	London		GB	
Morris, Philip	Surrey		GB	

US-CL-CURRENT: [713/201](#); [709/224](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWMC	Draw Desc	Image
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☐ 2. Document ID: US 20050091438 A1

L7: Entry 2 of 39

File: PGPB

Apr 28, 2005

PGPUB-DOCUMENT-NUMBER: 20050091438

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050091438 A1

TITLE: Exporting 12C controller interfaces for 12C slave devices using IPMI micro-controller

PUBLICATION-DATE: April 28, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chatterjee, Ranen	Fremont	CA	US	

US-CL-CURRENT: [710/315](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWMC	Draw Desc	Image
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☐ 3. Document ID: US 20050077921 A1

L7: Entry 3 of 39

File: PGPB

Apr 14, 2005

PGPUB-DOCUMENT-NUMBER: 20050077921
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050077921 A1

TITLE: Computer data bus interface control

PUBLICATION-DATE: April 14, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Percer, Benjamin Thomas	Roseville	CA	US	
Cherniski, Andrew Michael	Rescue	CA	US	

US-CL-CURRENT: 326/86

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 4. Document ID: US 20050060463 A1

L7: Entry 4 of 39

File: PGPB

Mar 17, 2005

PGPUB-DOCUMENT-NUMBER: 20050060463
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050060463 A1

TITLE: Management methods and apparatus that are independent of operating systems

PUBLICATION-DATE: March 17, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Le, Tuan A.	San Jose	CA	US	
Rinaldo, Christopher J.	San Jose	CA	US	
Mukherjee, Angshuman	Fremont	CA	US	
Truong, Vinh N.	San Jose	CA	US	
Delfatti, Daniel	Belmont	CA	US	

US-CL-CURRENT: 710/300

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 5. Document ID: US 20050041684 A1

L7: Entry 5 of 39

File: PGPB

Feb 24, 2005

PGPUB-DOCUMENT-NUMBER: 20050041684
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050041684 A1

TITLE: Multi-channel network monitoring apparatus, signal replicating device, and systems including such apparatus and devices, and enclosure for multi-processor equipment

PUBLICATION-DATE: February 24, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Reynolds, Alastair	Linlithgow	CO	GB	
Carson, Douglas John	Englewood		US	
Lunn, George Crowther	West Lothian		GB	
MacIsaac, William Ross	Dunfermline		GB	

US-CL-CURRENT: 370/463

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 6. Document ID: US 20040246982 A1

L7: Entry 6 of 39

File: PGPB

Dec 9, 2004

PGPUB-DOCUMENT-NUMBER: 20040246982

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040246982 A1

TITLE: Methods and apparatus for configuring a packet switching (PS) backplane to support various configurations

PUBLICATION-DATE: December 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Krishnamurthy, Ramani	Fremont	CA	US	
Ho, Raymond K.	San Jose	CA	US	
Sidhu, Balkar S.	San Jose	CA	US	

US-CL-CURRENT: 370/422

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 7. Document ID: US 20040225802 A1

L7: Entry 7 of 39

File: PGPB

Nov 11, 2004

PGPUB-DOCUMENT-NUMBER: 20040225802

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040225802 A1

TITLE: Supporting non-hotswap 64-bit CPCI cards in a HA system

PUBLICATION-DATE: November 11, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Krishnamurthy, Ramani	Fremont	CA	US	
Susarla, Srinivas	Fremont	CA	US	

US-CL-CURRENT: 710/302

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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L7: Entry 8 of 39

File: PGPB

Jul 8, 2004

PGPUB-DOCUMENT-NUMBER: 20040133819

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040133819 A1

TITLE: System and method for providing a persistent power mask

PUBLICATION-DATE: July 8, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Krishnamurthy, Viswanath	Sunnyvale	CA	US	
Delfatti, Daniel	Belmont	CA	US	

US-CL-CURRENT: 713/300

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 9. Document ID: US 20040117681 A1

L7: Entry 9 of 39

File: PGPB

Jun 17, 2004

PGPUB-DOCUMENT-NUMBER: 20040117681

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040117681 A1

TITLE: Methods and apparatus for providing microprocessor firmware control of power sequencing on a CPCI card

PUBLICATION-DATE: June 17, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mahony, Maire	Sunnyvale	CA	US	
Pelissier, Gerald	Round Rock	TX	US	

US-CL-CURRENT: 713/330

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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File: PGPB

Jun 17, 2004

PGPUB-DOCUMENT-NUMBER: 20040117431

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040117431 A1

TITLE: Mapping of hot-swap states to plug-in unit states

PUBLICATION-DATE: June 17, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Le, Tuan A.	San Jose	CA	US	
Rinaldo, Christopher J.	San Jose	CA	US	
Mukherjee, Angshuman	Fremont	CA	US	
Truong, Vinh H.	San Jose	CA	US	
Delfatti, Daniel	Belmont	CA	US	

US-CL-CURRENT: 709/200

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 11. Document ID: US 20040059862 A1

L7: Entry 11 of 39

File: PGPB

Mar 25, 2004

PGPUB-DOCUMENT-NUMBER: 20040059862

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040059862 A1

TITLE: Method and apparatus for providing redundant bus control

PUBLICATION-DATE: March 25, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Chan, Johni	Rancho Santa Fe	CA	US	

US-CL-CURRENT: [710/316](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 12. Document ID: US 20030140190 A1

L7: Entry 12 of 39

File: PGPB

Jul 24, 2003

PGPUB-DOCUMENT-NUMBER: 20030140190

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030140190 A1

TITLE: Auto-SCSI termination enable in a CPCI hot swap system

PUBLICATION-DATE: July 24, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mahony, Maire	Santa Clara	CA	US	
Pelissier, Gerald R.	Round Rock	TX	US	

US-CL-CURRENT: [710/302](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 13. Document ID: US 20030101426 A1

L7: Entry 13 of 39

File: PGPB

May 29, 2003

PGPUB-DOCUMENT-NUMBER: 20030101426

PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030101426 A1

TITLE: System and method for providing isolated fabric interface in high-speed network switching and routing platforms

PUBLICATION-DATE: May 29, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sarkinen, Scott A.	Mounds View	MN	US	
Swart, Jeffrey D.	Eden Prairie	MN	US	
Schlegel, Neil A.	Lino Lakes	MN	US	
Meyer, Jerome M.	Chanhassen	MN	US	
Hollinrake, David L.	Brooklyn Park	MN	US	

US-CL-CURRENT: 716/12

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWMC	Draw Desc	Image
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☐ 14. Document ID: US 20030075984 A1

L7: Entry 14 of 39

File: PGPB

Apr 24, 2003

PGPUB-DOCUMENT-NUMBER: 20030075984
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030075984 A1

TITLE: System for distributing power in CPCI computer architecture

PUBLICATION-DATE: April 24, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Creason, Richard R.	Palo Alto	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	

US-CL-CURRENT: 307/43

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWMC	Draw Desc	Image
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☐ 15. Document ID: US 20030074513 A1

L7: Entry 15 of 39

File: PGPB

Apr 17, 2003

PGPUB-DOCUMENT-NUMBER: 20030074513
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030074513 A1

TITLE: Bus communication architecture, in particular for multicomputing systems

PUBLICATION-DATE: April 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Grouzdev, Vladimir	Saint Germain-En-Laye		FR	

US-CL-CURRENT: 710/306

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 16. Document ID: US 20030023802 A1

L7: Entry 16 of 39

File: PGPB

Jan 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030023802

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030023802 A1

TITLE: Computer system having a hot swappable hot swap controller

PUBLICATION-DATE: January 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	

US-CL-CURRENT: 710/302; 307/1, 307/38, 361/139, 361/32

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 17. Document ID: US 20020196794 A1

L7: Entry 17 of 39

File: PGPB

Dec 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020196794

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020196794 A1

TITLE: Method and apparatus for centralized maintenance system within a distributed telecommunications architecture

PUBLICATION-DATE: December 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Bloch, Jack	Boca Raton	FL	US	
Phung, Van P. T.	Coral Springs	FL	US	
Laxman, Amruth	Boca Raton	FL	US	
Dinh, Le Van	Boca Raton	FL	US	

US-CL-CURRENT: 370/401; 370/389

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 18. Document ID: US 20020196611 A1

L7: Entry 18 of 39

File: PGPB

Dec 26, 2002

PGPUB-DOCUMENT-NUMBER: 20020196611

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020196611 A1

TITLE: RELIABLE CARD DETECTION IN A CPCI SYSTEM

PUBLICATION-DATE: December 26, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	

US-CL-CURRENT: 361/752

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 19. Document ID: US 20020191616 A1

L7: Entry 19 of 39

File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020191616

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020191616 A1

TITLE: Method and apparatus for a messaging protocol within a distributed telecommunications architecture

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sarmiento, Jesus L.	Miami	FL	US	
Bloch, Jack	Boca Raton	FL	US	
Laxman, Amruth	Boca Raton	FL	US	

US-CL-CURRENT: 370/400; 370/465, 370/522

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 20. Document ID: US 20020181194 A1

L7: Entry 20 of 39

File: PGPB

Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020181194

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020181194 A1

TITLE: Computer bus rack having an increased density of card slots

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	
Creason, Richard R.	Palo Alto	CA	US	

US-CL-CURRENT: 361/684; 361/683, 361/724

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KIMC	Draw Desc	Image
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File: PGPB

Apr 17, 2003

PGPUB-DOCUMENT-NUMBER: 20030074513

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030074513 A1

TITLE: Bus communication architecture, in particular for multicomputing systems

PUBLICATION-DATE: April 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Grouzdev, Vladimir	Saint Germain-En-Laye		FR	

APPL-NO: 10/ 192759 [\[PALM\]](#)

DATE FILED: July 10, 2002

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
FR	0109166	2001FR-0109166	July 10, 2001

INT-CL: [07] [G06](#) [F](#) [13/36](#)

US-CL-PUBLISHED: 710/306

US-CL-CURRENT: [710/306](#)

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A computer system comprises first and second computer boards, each having a processor, onboard memory, an onboard bus, e.g. a processor bus, and a bus-to-bus bridge for interconnecting the onboard bus with an external bus; the boards have remote slave drivers, and communication drivers, comprising communication management functions, and forming communication chains or channels between the remote slave drivers and the onboard memories.

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File: PGPB

Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020181194

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020181194 A1

TITLE: Computer bus rack having an increased density of card slots

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	
Creason, Richard R.	Palo Alto	CA	US	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	COUNTRY	TYPE CODE
SUN MICROSYSTEMS, INC.				02

APPL-NO: 09/ 873825 [\[PALM\]](#)

DATE FILED: June 4, 2001

INT-CL: [07] [G06 F 1/16](#)US-CL-PUBLISHED: [361/684](#); [361/683](#), [361/724](#)US-CL-CURRENT: [361/684](#); [361/683](#), [361/724](#)

REPRESENTATIVE-FIGURES: 12A

ABSTRACT:

A computer bus rack includes at least one circuit board. The circuit board has an increased density of add-on card slots, with the at least one circuit board having a front side and a back side, and the rack comprising a first plurality of slots coupled to the front side, and a second plurality of slots coupled to the back side. The first and second plurality of slots are arranged such that corresponding ones of the first and second slots are in substantial alignment, respectively. Also provided are a plurality of connectors having respective connector-pins extended in a direction substantially perpendicular to and away from the circuit board and having a column and row arrangement within the connectors. The connectors are affixed to the circuit board in alignment with the first and second plurality of slots, and each one of the plurality of connectors has connector-pins that are physically distinct from connector-pins of connectors of the other slots. Note that the slots on the front side and the back side are adapted to mate with add-on cards so as to increase the amount of add-on slots for a given form factor.

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File: PGPB

Dec 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020191616

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020191616 A1

TITLE: Method and apparatus for a messaging protocol within a distributed telecommunications architecture

PUBLICATION-DATE: December 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sarmiento, Jesus L.	Miami	FL	US	
Bloch, Jack	Boca Raton	FL	US	
Laxman, Amruth	Boca Raton	FL	US	

APPL-NO: 10/ 109128 [PALM]

DATE FILED: March 28, 2002

RELATED-US-APPL-DATA:

Application is a non-provisional-of-provisional application 60/279279, filed March 28, 2001,
Application is a non-provisional-of-provisional application 60/279295, filed March 28, 2001,

INT-CL: [07] H04 L 12/56

US-CL-PUBLISHED: 370/400; 370/465, 370/522

US-CL-CURRENT: 370/400; 370/465, 370/522

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A method for message handling in a telecommunications system having a network services processor (NSP) for accessing, processing, and distributing telecommunications in conformance with a predefined signaling system and for distributing processing applications including call handling and routing to a plurality of platforms, each platform having a unique address and responds to application specific messages, the method comprising: connecting the plurality of platforms to local area networks (LANs), the plurality of platforms include packet managers (PMs) for accessing, processing, and distributing packetized call data over a packet network and a plurality of media control platforms (MCPs) for accessing, processing, and distributing media tasks (MCTs); connecting the LANs to a corresponding plurality of interconnect controllers (ICCs), each ICC for interfacing the NSP with the plurality of platforms through a corresponding LAN; and distributing application specific messages to the plurality of platforms via a message protocol (hiQ) having a message frame which encapsulates application specific messages within a standard LAN protocol.

CONTINUATION DATA

[0001] This application claims the benefit of priority under 35 U.S.C. 119(e) to two copending U.S. Patent Provisional Applications, Serial Nos. 60/279,295 and 60/279,279, both filed on Mar. 28, 2001, the contents of each of said applications being incorporated by reference herein.

[0002] This application is also related to the following U.S. Patent Applications: U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Distributed Architecture for a Telecommunications Software Switch; U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Distributed Architecture for a Telecommunications System; U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Method and Apparatus for Providing A Software Adaptation Layer in a Telecommunications System; U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Method and Apparatus for a Deriving a Standard MAC Address from A Physical Location; U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Method and Apparatus for A Centralized Maintenance System within a Distributed Telecommunications Architecture; and U.S. patent application Ser. No. _____ filed Mar. 28, 2002 entitled Method and Apparatus for Providing a Proprietary Data Interface in a Distributed Telecommunications System, the contents of each of said applications being incorporated by reference herein.

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File: USPT

Dec 28, 2004

US-PAT-NO: 6836811

DOCUMENT-IDENTIFIER: US 6836811 B2

TITLE: Front access only CPCI computer system

DATE-ISSUED: December 28, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ho; Raymond K.	San Jose	CA		
Creason; Richard R.	Palo Alto	CA		
Kermaani; Kaamel M.	Cupertino	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Santa Clara	CA			02

APPL-NO: 09/ 953503 [\[PALM\]](#)

DATE FILED: September 12, 2001

INT-CL: [07] [H05 K 7/10](#), [H01 R 12/16](#)

US-CL-ISSUED: 710/301; 710/105, 361/788

US-CL-CURRENT: [710/301](#); [361/788](#), [710/105](#)

FIELD-OF-SEARCH: 710/105, 710/300, 710/301, 710/302, 710/306, 710/307, 710/313, 710/314, 206/706, 206/707, 211/41.17, 312/223.1, 312/223.2, 361/752, 361/753, 361/788, 361/796, 361/803, 439/61, 439/78, 439/82, 174/262

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS.

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	4511950	April 1985	Bunner et al.	361/788
<input type="checkbox"/>	6128196	October 2000	Hoyle et al.	361/752
<input type="checkbox"/>	6356966	March 2002	Loach et al.	439/78
<input type="checkbox"/>	6456498	September 2002	Larson et al.	361/752
<input type="checkbox"/>	6526465	February 2003	Voth et al.	710/301
<input type="checkbox"/>	6578103	June 2003	Hill et al.	710/313
<input type="checkbox"/>	6646868	November 2003	Ho et al.	361/684

ART-UNIT: 2111

PRIMARY-EXAMINER: Dang; Khanh

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kowert & Goetzel, P.C. Kivlin; B. Noel

ABSTRACT:

A system and apparatus for a compact peripheral component interconnect (CPCI) computer system having exclusive front card access for both active and passive CPCI cards is provided. This system is further comprised of an active backplane with a front and rear side, a plurality of slots, each of these slots comprising of at least one connector and each of these connectors having a column and row arrangement of connector-pins, wherein individual ones of these connector-pins correspond to selected pairs of adjacent slots, and wherein selected adjacent slot pairs are reserved for particular pairs of CPCI cards comprising a single active card and a single passive card.

18 Claims, 9 Drawing figures

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☐ 31. Document ID: US 6646868 B2

L7: Entry 31 of 39

File: USPT

Nov 11, 2003

US-PAT-NO: 6646868

DOCUMENT-IDENTIFIER: US 6646868 B2

TITLE: Computer bus rack having an increased density of card slots

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMMC	Draw Desc	Image
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☐ 32. Document ID: US 6636917 B1

L7: Entry 32 of 39

File: USPT

Oct 21, 2003

US-PAT-NO: 6636917

DOCUMENT-IDENTIFIER: US 6636917 B1

TITLE: Card design having tape and disk drives

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMMC	Draw Desc	Image
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☐ 33. Document ID: US 6633835 B1

L7: Entry 33 of 39

File: USPT

Oct 14, 2003

US-PAT-NO: 6633835

DOCUMENT-IDENTIFIER: US 6633835 B1

TITLE: Prioritized data capture, classification and filtering in a network monitoring environment

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMMC	Draw Desc	Image
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☐ 34. Document ID: US 6614752 B1

L7: Entry 34 of 39

File: USPT

Sep 2, 2003

US-PAT-NO: 6614752

DOCUMENT-IDENTIFIER: US 6614752 B1

**** See image for Certificate of Correction ****

TITLE: Transitioning a standards-based card into a high availability backplane environment

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMMC	Draw Desc	Image
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☐ 35. Document ID: US 6608761 B2

L7: Entry 35 of 39

File: USPT

Aug 19, 2003

US-PAT-NO: 6608761

DOCUMENT-IDENTIFIER: US 6608761 B2

**** See image for Certificate of Correction ****

TITLE: Multiple processor cards accessing common peripherals via transparent and non-transparent bridges

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 36. Document ID: US 6501660 B1

L7: Entry 36 of 39

File: USPT

Dec 31, 2002

US-PAT-NO: 6501660

DOCUMENT-IDENTIFIER: US 6501660 B1

TITLE: Reliable card detection in a CPCI system

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 37. Document ID: US 6418026 B1

L7: Entry 37 of 39

File: USPT

Jul 9, 2002

US-PAT-NO: 6418026

DOCUMENT-IDENTIFIER: US 6418026 B1

TITLE: Bus rack for accommodating plural stand-alone computers

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 38. Document ID: US 6341068 B1

L7: Entry 38 of 39

File: USPT

Jan 22, 2002

US-PAT-NO: 6341068

DOCUMENT-IDENTIFIER: US 6341068 B1

TITLE: Low profile connector system for providing multiple drives on a card

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 39. Document ID: US 6289376 B1

L7: Entry 39 of 39

File: USPT

Sep 11, 2001

US-PAT-NO: 6289376

DOCUMENT-IDENTIFIER: US 6289376 B1

TITLE: Tightly-coupled disk-to-CPU storage server

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	WMC	Draw Desc	Image
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US006836811B2

(12) **United States Patent**
Ho et al.

(10) Patent No.: **US 6,836,811 B2**
(45) Date of Patent: **Dec. 28, 2004**

(54) **FRONT ACCESS ONLY CPCI COMPUTER SYSTEM**

(73) **Inventors:** Raymond K. Ho, San Jose, CA (US);
Richard R. Crestoni, Palo Alto, CA (US);
Kassim M. Kermassani, Cupertino, CA (US)

(73) **Assignee:** Sun Microsystems, Inc., Santa Clara, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 457 days.

(21) Appl. No.: 09/923,583

(22) Filed: Sep. 12, 2001

(65) **Prior Publication Data**
US 2003/0051068 A1 Mar. 13, 2003

(31) Int. Cl.⁷ H05K 7/10; H01R 12/16

(52) U.S. Cl. 710/301; 710/105; 361/786

(58) **Field of Search** 710/105, 301, 710/301, 302, 304, 307, 313, 314, 364, 704, 707, 711, 712, 713, 714, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000

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- 6,579,073 B1 * 6/2003 Choi et al. 710/313
- 6,646,888 B2 * 11/2003 Ho et al. 361/684

* cited by examiner

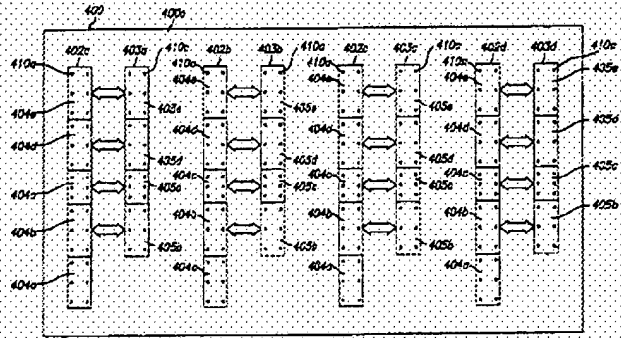
Primary Examiner—Khash Ding

(74) Attorney, Agent, or Firm—Maymone Hood Kivlin Kowert & Costello, P.C.; B. Noll Kivlin

(57) **ABSTRACT**

A system and apparatus for a compact peripheral component interconnect (CPCI) computer system having exclusive front card access for both active and passive CPCI cards is provided. This system is further comprised of an active backplane with a front and rear side, a plurality of slots, each of these slots comprising of at least one connector and each of these connectors having a column and row arrangement of connector pins, wherein individual ones of these connector pins correspond to selected pairs of adjacent slots, and wherein selected adjacent slot pairs are reserved for particular pairs of CPCI cards comprising a single active card and a single passive card.

18 Claims, 6 Drawing Sheets





US06618783B1

(12) **United States Patent**
Hammersley

(10) Patent No.: **US 6,618,783 B1**
(45) Date of Patent: **Sep. 9, 2003**

(54) **METHOD AND SYSTEM FOR MANAGING A PCI BUS COUPLED TO ANOTHER SYSTEM**

(75) Inventor: **Peter J. Hammersley, San Jose, CA (US)**

(73) Assignee: **Hewlett-Packard Development Company, L.P., Houston, TX (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/430,369

(22) Filed: Oct. 29, 1999

(51) Int. Cl.: G06F 13/14

(52) U.S. Cl.: 718/304; 718/110

(58) Field of Search: 718/300, 301, 718/302, 303, 304, 305, 306; 714/76, 11, 13, 14, 41

(55) References Cited

U.S. PATENT DOCUMENTS

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6,112,371 A * 8/2000 Laine et al. 718/306
6,118,247 A * 10/2000 McKay et al. 716/10
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6,229,721 B1 * 12/2000 Hsi et al. 718/302
6,351,432 B1 * 2/2001 Koenig et al. 120/217
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* cited by examiner

Primary Examiner—Samuel L. Gervais

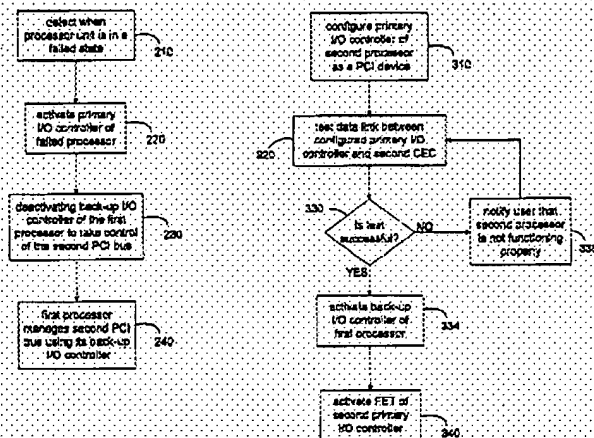
Assistant Examiner—M. Chang-Tsai

(74) Attorney, Agent, or Firm—David M. Mason

(57) ABSTRACT

The present invention provides a PCI bus switching architecture to allow a pair of PCI processors to have access to a common set of PCI I/O cards. More specifically, this design allows either core-coupled processor to dynamically take over the operational control of the common set of PCI I/O cards if the primary processor for the same becomes inoperative. The present invention achieves the objective by employing a point to point data link connection between each processor and their respective controllers for each common set of PCI I/O cards associated with a PCI bus.

10 Claims, 4 Drawing Sheets



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☐ 1. Document ID: US 20050060463 A1

L4: Entry 1 of 22

File: PGPB

Mar 17, 2005

PGPUB-DOCUMENT-NUMBER: 20050060463

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050060463 A1

TITLE: Management methods and apparatus that are independent of operating systems

PUBLICATION-DATE: March 17, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Le, Tuan A.	San Jose	CA	US	
Rinaldo, Christopher J.	San Jose	CA	US	
Mukherjee, Angshuman	Fremont	CA	US	
Truong, Vinh N.	San Jose	CA	US	
Delfatti, Daniel	Belmont	CA	US	

US-CL-CURRENT: [710/300](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 2. Document ID: US 20040141285 A1

L4: Entry 2 of 22

File: PGPB

Jul 22, 2004

PGPUB-DOCUMENT-NUMBER: 20040141285

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040141285 A1

TITLE: Modular computer system with passive backplane modules

PUBLICATION-DATE: July 22, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lefebvre, Jean-Pierre	Boisbriand		CA	
Muraglia, Philippe	Boisbriand		CA	
Belair, Rick	Terrebonne		CA	
Adam, Yan	Sainte-Therese		CA	

US-CL-CURRENT: [361/683](#)

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 3. Document ID: US 20040088463 A1

L4: Entry 3 of 22

File: PGPB

May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040088463

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040088463 A1

TITLE: System and method for DHCP client-ID generation

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Krishnamurthy, Viswanath	Sunnyvale	CA	US	
Hyder, Mir J.	Sunnyvale	CA	US	
Jain, Sunit	Fremont	CA	US	

US-CL-CURRENT: 710/301; 710/104

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 4. Document ID: US 20030185231 A1

L4: Entry 4 of 22

File: PGPB

Oct 2, 2003

PGPUB-DOCUMENT-NUMBER: 20030185231

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030185231 A1

TITLE: Telephony data to host streaming via a computer interface

PUBLICATION-DATE: October 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dobler, Steven R.	Stanhope	NJ	US	

US-CL-CURRENT: 370/465; 370/352

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 5. Document ID: US 20030086421 A1

L4: Entry 5 of 22

File: PGPB

May 8, 2003

PGPUB-DOCUMENT-NUMBER: 20030086421

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030086421 A1

TITLE: Multiple-domain processing system using hierarchically orthogonal switching fabric

PUBLICATION-DATE: May 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Awsienko, Oleg	Phoenix	AZ	US	
Butler, Edward	Chandler	AZ	US	
McAlpine, Gary L.	Banks	OR	US	
Minturn, David B.	Hillsboro	OR	US	
Schaefer, Joseph	Chandler	AZ	US	
Solomon, Gary A.	Acton	MA	US	

US-CL-CURRENT: 370/387; 370/400, 709/218

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 6. Document ID: US 20030074513 A1

L4: Entry 6 of 22

File: PGPB

Apr 17, 2003

PGPUB-DOCUMENT-NUMBER: 20030074513

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030074513 A1

TITLE: Bus communication architecture, in particular for multicomputing systems

PUBLICATION-DATE: April 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Grouzdev, Vladimir	Saint Germain-En-Laye		FR	

US-CL-CURRENT: 710/306

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 7. Document ID: US 20030056049 A1

L4: Entry 7 of 22

File: PGPB

Mar 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030056049

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030056049 A1

TITLE: High speed serial data transport between communications hardware modules

PUBLICATION-DATE: March 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kaku, Vicky B.	San Diego	CA	US	

US-CL-CURRENT: 710/300

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw Desc	Image
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☐ 8. Document ID: US 20030051088 A1

L4: Entry 8 of 22

File: PGPB

Mar 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030051088

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030051088 A1

TITLE: Front access only CPCI computer system

PUBLICATION-DATE: March 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Creason, Richard R.	Palo Alto	CA	US	
Kermaani, Kaamel M.	Cupertino	CA	US	

US-CL-CURRENT: 710/300

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 9. Document ID: US 20020186712 A1

L4: Entry 9 of 22

File: PGPB

Dec 12, 2002

PGPUB-DOCUMENT-NUMBER: 20020186712

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020186712 A1

TITLE: Method and apparatus for providing a software adaption layer in a telecommunications system

PUBLICATION-DATE: December 12, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dinh, Le Van	Boca Raton	FL	US	
Laxman, Amruth	Boca Raton	FL	US	
Sarmiento, Jesus L.	Miami	FL	US	

US-CL-CURRENT: 370/469; 370/465

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 10. Document ID: US 20020181194 A1

L4: Entry 10 of 22

File: PGPB

Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020181194

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020181194 A1

TITLE: Computer bus rack having an increased density of card slots

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ho, Raymond K.	San Jose	CA	US	
Jochiong, Victor E.	Mill Valley	CA	US	
Creason, Richard R.	Palo Alto	CA	US	

US-CL-CURRENT: 361/684; 361/683, 361/724

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWC	Draw Desc	Image
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☐ 11. Document ID: US 20020093966 A1

L4: Entry 11 of 22

File: PGPB

Jul 18, 2002

PGPUB-DOCUMENT-NUMBER: 20020093966

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020093966 A1

TITLE: Enhanced CMTS for reliability, availability, and serviceability

PUBLICATION-DATE: July 18, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Liva, Valentino	Los Altos	CA	US	
Sharma, Alok	San Jose	CA	US	
Smith, Lance	San Jose	CA	US	
Yee, James	Union City	CA	US	

US-CL-CURRENT: 370/400; 370/465

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 12. Document ID: US 20020012232 A1

L4: Entry 12 of 22

File: PGPB

Jan 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020012232

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020012232 A1

TITLE: Computer system having front and rear cable access

PUBLICATION-DATE: January 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Creason, Richard	Palo Alto	CA	US	
Willis, Clifford B.	Tracy	CA	US	
Silverman, Denise	San Carlos	CA	US	
White, Michael Sean	San Jose	CA	US	
Arstein, David M.	Scotts Valley	CA	US	
JoChiong, Victor E.	Mill Valley	CA	US	
Mautz, Timothy E.	San Francisco	CA	US	
Wilson, Steve M.	San Jose	CA	US	
Ho, Raymond Kai	San Jose	CA	US	

Kermaani, Kaamel	Cupertino	CA	US
Meert, Carl	Sunnyvale	CA	US
Bigio, Adiyamar	Scotts Valley	CA	US
Hileman, Vince	Sunnyvale	CA	US

US-CL-CURRENT: 361/727; 361/683, 361/724, 361/725

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	Image
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☐ 13. Document ID: US 6865637 B1

L4: Entry 13 of 22

File: USPT

Mar 8, 2005

US-PAT-NO: 6865637

DOCUMENT-IDENTIFIER: US 6865637 B1

TITLE: Memory card and system for updating distributed memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	Image
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☐ 14. Document ID: US 6847652 B1

L4: Entry 14 of 22

File: USPT

Jan 25, 2005

US-PAT-NO: 6847652

DOCUMENT-IDENTIFIER: US 6847652 B1

TITLE: Bus control module for a multi-stage clock distribution scheme in a signaling server

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	Image
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☐ 15. Document ID: US 6836811 B2

L4: Entry 15 of 22

File: USPT

Dec 28, 2004

US-PAT-NO: 6836811

DOCUMENT-IDENTIFIER: US 6836811 B2

TITLE: Front access only CPCI computer system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	Image
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☐ 16. Document ID: US 6662254 B1

L4: Entry 16 of 22

File: USPT

Dec 9, 2003

US-PAT-NO: 6662254

DOCUMENT-IDENTIFIER: US 6662254 B1

TITLE: System architecture

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMMC	Draw Desc	Image
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☐ 17. Document ID: US 6636917 B1

L4: Entry 17 of 22

File: USPT

Oct 21, 2003

US-PAT-NO: 6636917

DOCUMENT-IDENTIFIER: US 6636917 B1

TITLE: Card design having tape and disk drives

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 18. Document ID: US 6608761 B2

L4: Entry 18 of 22

File: USPT

Aug 19, 2003

US-PAT-NO: 6608761

DOCUMENT-IDENTIFIER: US 6608761 B2

**** See image for Certificate of Correction ****TITLE: Multiple processor cards accessing common peripherals via transparent and non-transparent bridges

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 19. Document ID: US 6578103 B1

L4: Entry 19 of 22

File: USPT

Jun 10, 2003

US-PAT-NO: 6578103

DOCUMENT-IDENTIFIER: US 6578103 B1

TITLE: Compact PCI backplane and method of data transfer across the compact PCI backplane

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 20. Document ID: US 6515985 B2

L4: Entry 20 of 22

File: USPT

Feb 4, 2003

US-PAT-NO: 6515985

DOCUMENT-IDENTIFIER: US 6515985 B2

TITLE: Convergence of telephone signaling, voice and data over a packet-switched network

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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